PIC16F636/639

PIC16F636/639 Rev. A Silicon/Data Sheet Errata

The PIC16F636/639 parts you have received conform functionally to the Device Data Sheet (DS41232**B**), except for the anomalies described below.

Microchip intends to address all issues listed here in future revisions of the **PIC16F636/639** devices.

1. Module: Resets (when WDT times out)

If the OPTION_REG bits: PS<2:0> are changed from any other value to '000', multiple spurious Resets can occur when the WDT times out. These Resets can occur even when the PSA bit is clear, assigning the prescaler to the Timer0.

Work around

If a CLRWDT instruction is issued before the WDT times out and before the OPTION register PS<2:0> bits are modified, this problem is eliminated.

Date Codes that pertain to this issue:

All engineering and production devices.

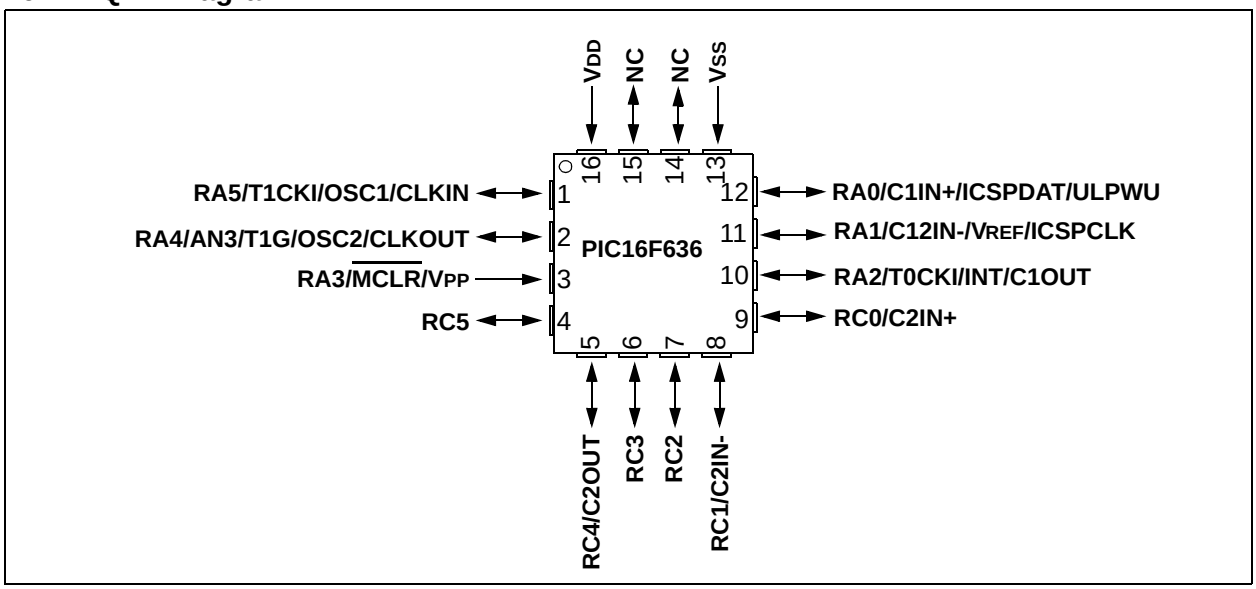
Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41232**B**), the following clarifications and corrections should be noted.

1. Module: New 4x4 QFN Package Added

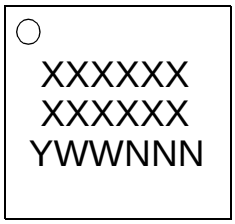
The new 16-pin 4x4 QFN pinout diagrams will be added to the Pin Diagrams figure on page 2 and the Packaging Information chapter as shown below:

16-Pin QFN Diagram

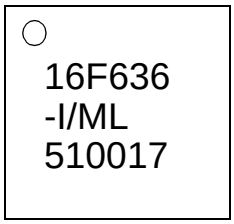


14.1 Package Marking Information

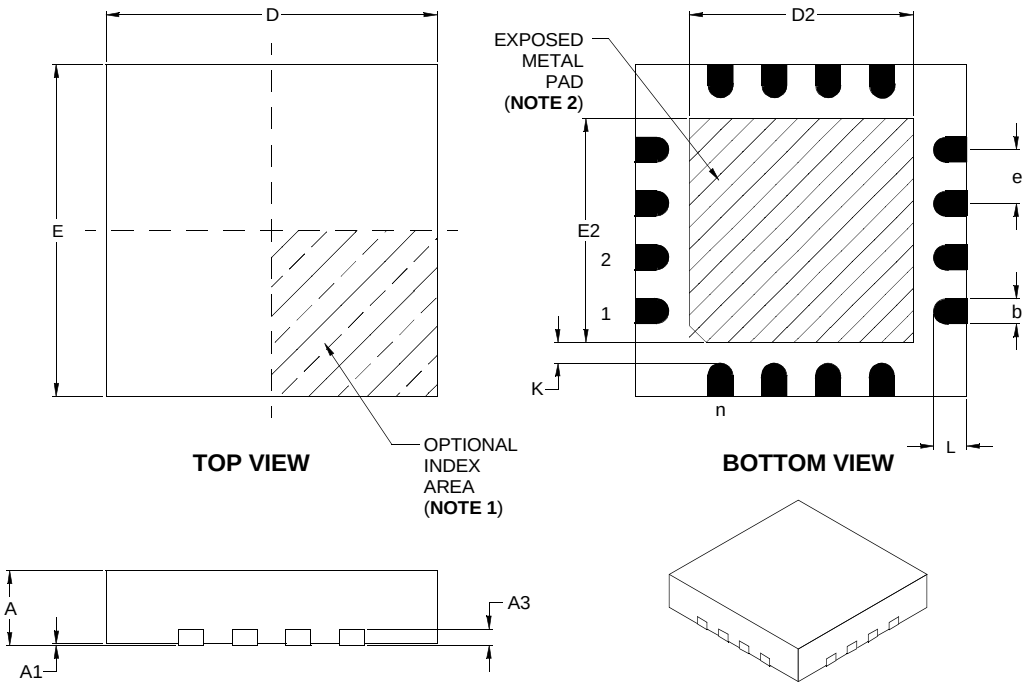
16-Lead QFN



Example



16-Lead Plastic Quad Flat No Lead Package (ML) 4x4x0.9 mm Body (QFN) – Saw Singulated



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		16			16	
Pitch	e		.026 BSC			0.65 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3		.008 REF			0.20 REF	
Overall Width	E	.152	.157	.163	3.85	4.00	4.15
Exposed Pad Width	E2	.090**	–	.110	2.29**	–	2.80
Overall Length	D	.152	.157	.163	3.85	4.00	4.15
Exposed Pad Length	D2	.090	–	.110	2.29	–	2.80
Contact Width	b	.010	.012	.014	0.25	0.30	0.35
Contact Length §	L	.012	.016	.020	0.30	0.40	0.50
Contact-to-Exposed Pad §	K	.008	–	–	0.20	–	–

***** Controlling Parameter

****** Outside JEDEC Specification

§ Significant Characteristic

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Exposed pad varies according to die attach paddle size.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

JEDEC equivalent: M0-220 VGGC-3

Drawing No. C04-127

Revised 09-13-05

2. Module: I/O Pins

Register 4-1 should be titled “WDA – Weak Pull-up/Pull-down Direction Register”. Register 4-2 should be titled “WPUDA – Weak Pull-up/Pull-down Enable Register”, as shown below.

REGISTER 14-1: WDA: WEAK PULL-UP/PULL-DOWN DIRECTION REGISTER (ADDRESS: 97h)

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0
bit 7							bit 0

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-4 **WDA<5:4>**: Pull-up/Pull-down Selection bits
1 = Pull-up selected
0 = Pull-down selected

bit 3 **Unimplemented**: Read as ‘0’

bit 2-0 **WDA<2:0>**: Pull-up/Pull-down Selection bits
1 = Pull-up selected
0 = Pull-down selected

Note 1: The weak pull-up/pull-down device is enabled only when the global $\overline{\text{RAPU}}$ bit is enabled, the pin is in Input mode (TRIS = 1), the individual WDA bit is enabled (WDA = 1) and the pin is not configured as an analog input or clock function.

2: RA3 pull-up is enabled when the pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register and the device is not in Programming mode.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 14-2: WPUDA: WEAK PULL-UP/PULL-DOWN ENABLE REGISTER (ADDRESS: 95h)

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPUDA5(3)	WPUDA4(3)	—	WPUDA2	WPUDA1	WPUDA0
bit 7							bit 0

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-4 **WPUDA<5:4>**: Pull-up/Pull-down Direction Selection bits(3)
1 = Pull-up/pull-down enabled
0 = Pull-up/pull-down disabled

bit 3 **Unimplemented**: Read as ‘0’

bit 2-0 **WPUDA<2:0>**: Pull-up/Pull-down Direction Selection bits
1 = Pull-up/pull-down enabled
0 = Pull-up/pull-down disabled

Note 1: The weak pull-up/pull-down direction device is enabled only when the global $\overline{\text{RAPU}}$ bit is enabled, the pin is in Input mode (TRIS = 1), the individual WPUDA bit is enabled (WPUDA = 1) and the pin is not configured as an analog input or clock function.

2: RA3 pull-up is enabled when the pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register and the device is not in Programming mode.

3: WPUDA5 bit can be written if INTOSC is enabled and T1OSC is disabled; otherwise, the bit can not be written and reads as ‘1’. WPUDA4 bit can be written if not configured as OSC2; otherwise, the bit can not be written and reads as ‘1’.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

3. Module: Data EEPROM Memory

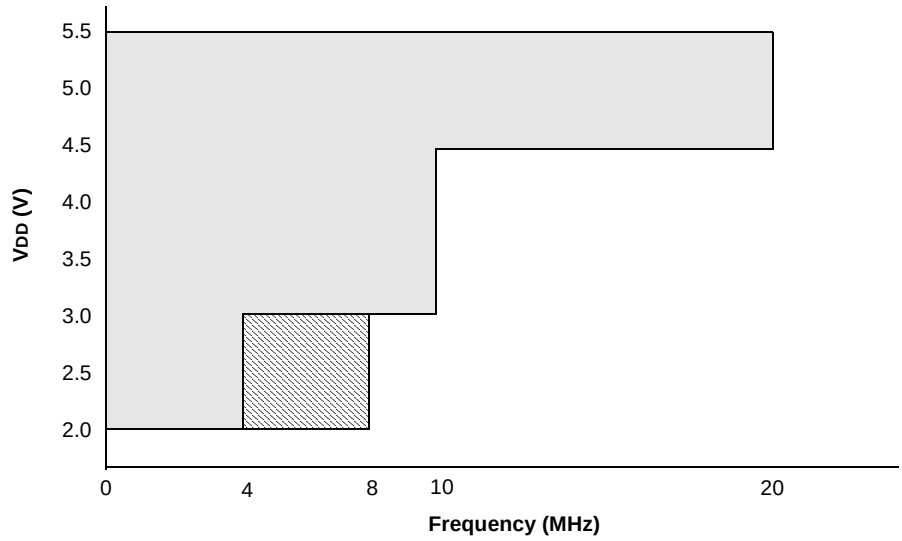
In Section 9.0, paragraph 2, the number of bytes for PIC12F635 should be 128 (as shown in bold).

EEDAT holds the 8-bit data for read/write and EEADR holds the address of the EEPROM location being accessed. PIC16F636/639 has 256 bytes of data EEPROM and the PIC12F635 has **128** bytes.

4. Module: Electrical Specifications

Figure 15-1, “PIC12F635/PIC16F636 Voltage Frequency Graph, -40C Ta +125C”, and Figure 15-2, “PIC16F639 Voltage Frequency Graph, -40C Ta +125C” should read as follows:

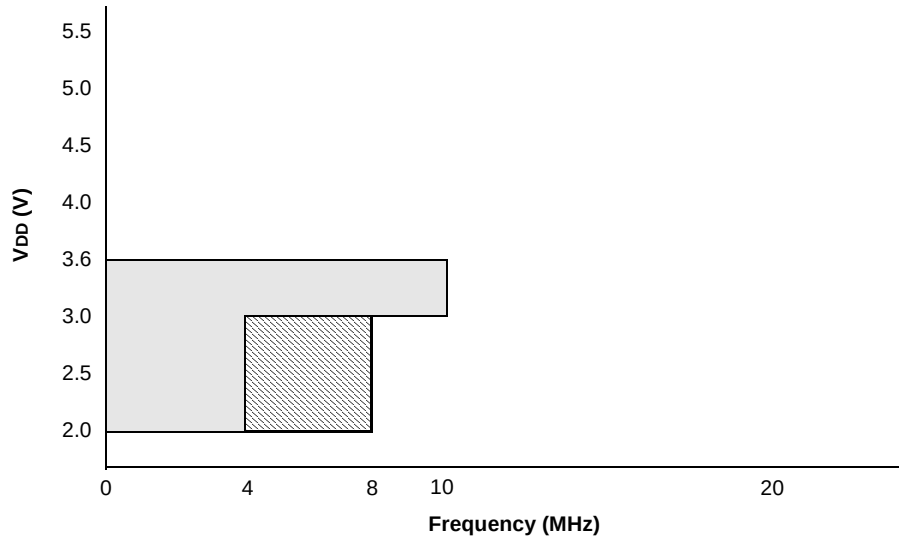
FIGURE 15-1: PIC12F635/16F636 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: Cross-hatched area is for HFINTOSC and EC modes only.

FIGURE 15-2: PIC16F639 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: Cross-hatched area is for HFINTOSC and EC modes only.

In Section 15.1: “DC Characteristics”, the Supply Voltage conditions for parameter D001 should be “8 MHz: HFINTOSC, EC” as shown in the table below.

15.2 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) PIC12F635/PIC16F636-E (Extended)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**	2.0	—	5.5	V	FOSC < = **8 MHz: HFINTOSC, EC**
D001			2.0	—	5.5	V	FOSC < = 4 MHz
D001C			3.0	—	5.5	V	FOSC < = 10 MHz
D001D			4.5	—	5.5	V	FOSC < = 20 MHz
D002	VDR	**RAM Data Retention Voltage(1)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See **Section 12.3 “Power-on Reset”** for details.
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See **Section 12.3 “Power-on Reset”** for details.
D005	VBOD	**Brown-out Detect**	—	2.1	—	V	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

REVISION HISTORY

Rev A Document (8/2004)
Issue 1 – When OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out.

Added Clarifications/Corrections to the Data Sheet, Issues 1, 2 and 3 (changed to 8-pin MF **saw singulated** packaging).

Rev B Document (01/2005)

Added PIC16F639 device.

Revised Module 1: Resets.

Deleted Clarification/Corrections to the Data Sheet. Data Sheet has been updated.

Rev C Document (07/2005)

Data Sheet Clarifications/Corrections Section: Added Module 1: New 4x4 QFN Package added.

Rev D Document (02/2006)

Data Sheet Clarifications/Corrections Section: Added Module 2: I/O Pins.

Rev E Document (03/2006)

Data Sheet Clarifications/Corrections section: Added Module 3: Data EEPROM Memory; Added Module 4: Electrical Specifications. Replaced QFN Package Drawing.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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